Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (currently amended): An apparatus to tune a tunable Gm-C circuit, the apparatus comprising:

a master Gm-C circuit comprising a transconductance and a tunable element, wherein the master Gm-C circuit is configured to provide a waveform that is dependent on a tuning signal applied to the tunable element;

a first signal generator to generate ~~provide~~ a ~~precision~~ first clock signal;

a second signal generator to provide a second clock signal to the master Gm-C circuit;

a sampler having a first input coupled to receive the waveform from the master Gm-C circuit, ~~and~~ a second input coupled to receive the ~~precision~~ first clock signal, a third input coupled to receive the second clock signal, and an output to provide a tuning error signal; and

a tuning control stage having an input coupled to the output of the sampler and having an output to provide the tuning signal to the master Gm-C circuit and to the tunable Gm-C circuit.

Claim 2 (currently amended): An apparatus as defined in Claim 1, wherein the tuning error signal is dependent upon a relationship between the first clock signal ~~generator~~ and the waveform provided by the master Gm-C circuit.

Claim 3 (previously presented): An apparatus as defined in Claim 2, wherein the tuning error signal assumes a first value in response to a value of the waveform in a first direction and assumes a second value in response to a value of the waveform in a second direction.

Claim 4 (previously presented) An apparatus as defined in Claim 1, further comprising a comparator coupled between the master Gm-C circuit and the sampler.

Claims 5-7 (cancel)

Claim 8 (previously presented): An apparatus as defined in Claim 1, wherein the tuning control stage is operative in response to the tuning error signal to adjust the tuning signal

in a first direction in response to a first value of the tuning error signal and to adjust the tuning signal in a second direction in response to a second value of the tuning error signal.

Claims 9-10 (cancel)

Claim 11 (previously presented): An apparatus as defined in Claim 8, wherein the tuning control stage is configured to provide, during tuning, a sequence of digital tuning signals, wherein the sequence of digital tuning signals converges to a final digital tuning signal that approximates an ideal digital tuning signal.

Claim 12 (previously presented): An apparatus as defined in Claim 11, wherein the tuning control stage is configured to provide a predetermined initial digital tuning signal at inception of the tuning and to provide subsequent sequential digital tuning signals in response to operation of the master Gm-C circuit.

Claims 13-30 (cancel)

Claim 31 (currently amended): A tuning apparatus comprising:

a waveform generator to provide a time-varying waveform, the waveform generator comprising a master controllable tuning element;

a first clock generator to control the waveform generator;

a second clock generator to provide a precision clock signal;

means responsive to the ~~time-varying waveform~~ precision clock signal for sampling the ~~precision clock signal~~ time-varying waveform; and

a tuning control stage coupled to the means for sampling to generate a corrected tuning signal in response to an output of the means for sampling, the corrected tuning signal to be provided to the master controllable tuning element and to a slave controllable tuning element, wherein the tuning control stage is to generate a reset signal to reset the waveform generator.

Claim 32 (original): A tuning apparatus as defined in Claim 31, wherein the master controllable tuning element is matched to the slave controllable tuning element.

Claim 33 (previously presented): A tuning apparatus as defined in Claim 31, wherein the sampling means comprises:

a first circuit to provide a binary output signal that has a value determined by the time-varying waveform; and

a second circuit coupled to the first circuit and to the second clock generator, the second circuit to provide a tuning error signal.

Claim 34 (original): A tuning apparatus as defined in Claim 33, wherein the tuning error signal assumes a first value in response to a tuning error in a first direction and assumes a second value in response to a tuning error in a second direction.

Claim 35 (original): A tuning apparatus as defined in Claim 33, wherein the first circuit comprises a comparator and the second circuit comprises a sampler.

Claim 36 (previously presented): A tuning apparatus as defined in Claim 35, wherein the comparator comprises a first input coupled to a reference voltage and a second input coupled to the waveform generator, wherein the comparator is to provide a comparator output signal determined by the relationship between the reference voltage and the time-varying waveform.

Claim 37 (cancel)

Claim 38 (previously presented): A tuning apparatus as defined in Claim 31, wherein the tuning control stage is configured to provide, during tuning, a sequence of digital tuning signals, wherein the sequence of digital tuning signals converges to a final digital tuning signal that approximates an ideal digital tuning signal.

Claim 39 (previously presented): A tuning apparatus as defined in Claim 38, wherein the tuning control stage is configured to provide a predetermined initial digital tuning signal at inception of the tuning and to provide subsequent sequential digital tuning signals in response to operation of the waveform generator.

Claims 40-42 (cancel)

Claim 43 (currently amended): A system comprising:

a low-noise amplifier (LNA) to receive a modulated carrier;

a mixer coupled to the LNA;

a demodulator coupled to the mixer;

a Gm-C filter coupled to the demodulator; and

an apparatus to tune the Gm-C filter, the apparatus comprising:

a waveform generator to provide a time-varying waveform, the waveform generator comprising a transconductance and a master controllable tuning element;

a first clock generator to provide a first clock signal;

a sampling circuit coupled to receive the first clock signal and a second clock signal, the sampling circuit responsive to the ~~time-varying waveform~~ first clock signal to sample the time-varying waveform; ~~clock signal; and~~

a second clock generator to provide the second clock signal to drive the waveform generator; and

a tuning control stage coupled to the sampling circuit to generate a tuning signal in response to an output of the sampling circuit, the tuning signal to be provided to the master controllable tuning element and to a slave controllable tuning element in the Gm-C filter.

Claim 44 (original): A tuning apparatus as defined in Claim 43, wherein the master controllable tuning element is matched to the slave controllable tuning element.

Claim 45 (currently amended): A tuning apparatus as defined in Claim 43, wherein the sampling circuit comprises:

a first circuit to provide a binary output signal that has a value determined by the relationship of the time-varying waveform to a reference voltage; and

a second circuit coupled to the first circuit and to the first clock generator, the second circuit to provide a tuning error signal.

Claim 46 (previously presented): A tuning apparatus as defined in Claim 45, wherein the tuning control stage is operative in response to the tuning error signal to control the tuning signal in a first direction in response to a first value of the tuning error signal and control the tuning signal in a second direction in response to a second value of the tuning error signal.

Claim 47 (original): A tuning apparatus as defined in Claim 46, wherein the tuning control stage is configured to provide, during the course of a tuning process, a sequence of digital

tuning signals, wherein the sequence of digital tuning signals converges to a final digital tuning signal that approximates an ideal digital tuning signal.

Claim 48 (currently amended): A tuning apparatus as defined in Claim 47, wherein the tuning stage is configured to provide a predetermined initial digital tuning signal at inception of the ~~control~~ tuning process and to provide subsequent sequential digital tuning signals in response to operation of the waveform generator.

Claim 49 (currently amended): A method comprising:

measuring a time period of a time-constant circuit including a master controllable tuning element under control of a first clock signal, wherein the time-constant circuit is coupled to a sampler that synchronizes the measure of the time period responsive to a second clock signal;

generating a tuning signal based on the measured time period and feeding the tuning signal back to the time-constant circuit until the measured time period reaches a desired value; and

providing ~~a value of~~ the tuning signal to a slave controllable transconductance.

Claim 50 (previously presented): A method as defined in Claim 49, further comprising controlling the master controllable tuning element with the tuning signal.

Claim 51 (previously presented): A method as defined in Claim 49, further comprising providing a predetermined initial digital tuning signal at inception of a tuning process and providing sequential digital tuning signals in response to the time period.

Claim 52 (previously presented): A method as defined in Claim 51, further comprising:

providing the sequential digital tuning signals until convergence at a final digital tuning signal that is provided to the slave controllable transconductance.

Claim 53 (previously presented): A method as defined in Claim 52, further comprising:

driving a counter with a clock signal that has a clock period related to an ideal tuning voltage for the master controllable tuning element.

Claim 54 (cancel)

Claim 55 (previously presented): The apparatus of Claim 1, wherein the tuning control stage comprises a convergence detector and a completion detector.

Claim 56 (previously presented): The apparatus of Claim 55, wherein the convergence detector is to detect toggling in the tuning signal and to generate a convergence output in response to the toggling.

Claim 57 (previously presented): The apparatus of Claim 55, wherein the completion detector is to detect completion of a tuning step by the tuning control stage and to generate a completion output in response to the completion.

Claim 58 (cancel)

Claim 59 (currently amended): The apparatus of Claim [[58]] 1, wherein the second signal generator is to reset the apparatus upon receipt of the convergence output.

Claim 60 (currently amended): The apparatus of Claim [[58]] 1, wherein the second signal generator is to reset the master Gm-C circuit upon receipt of the completion output.

Claim 61 (previously presented): The apparatus of Claim 1, further comprising a switch to selectively couple the transconductance to the tunable element.

Claim 62 (currently amended): An apparatus comprising:

a master circuit including a tunable element, wherein the master circuit is to generate a waveform based upon on a tuning signal;

a first signal generator to control operation of the master circuit;

a tuning controller ~~having an input based on~~ coupled to receive the waveform and having an output to provide the tuning signal to the master circuit and to a Gm-C filter, wherein the tuning controller comprises a convergence detector and a completion detector, wherein the first signal generator is to reset the apparatus upon receipt of a convergence output from the convergence detector and to reset the master circuit upon receipt of a completion output from the completion detector.

Claim 63 (cancel)

Claim 64 (currently amended): The apparatus of claim [[63]] 62, wherein the convergence detector is to detect toggling in the tuning signal and to generate [[a]] the convergence output in response to the toggling.

Claim 65 (currently amended): The apparatus of claim [[63]] 62, wherein the completion detector is to detect completion of a tuning step by the tuning controller and to generate [[a]] the completion output in response to the completion.

Claim 66 (previously presented): The apparatus of claim 62, wherein the master circuit further comprises a switch to selectively couple a transconductance to the tunable element.

Claim 67 (currently amended): The apparatus of claim [[63]] 62, wherein the convergence detector and the completion detector are coupled to the first signal generator.

Claims 68 – 69 (cancel)